CLAIMS

What is claimed is:

Claim 1. A system for decimal multiplication in a microprocessor comprising:

a recoder configured to recode decimal digits of a first operand to a corresponding set of {-5 to +5} and configured to recode decimal digits of a second operand to a corresponding set of {-5 to +5};

a multiplier array of digit multipliers, each digit multiplier configured to generate a partial product of a selected digit of a recoded first operand and a recoded second operand; and

an adder array of digit adders, each adder configured to generate a sum of said partial products, wherein a least significant digit of said sum is shifted to a results register, and each adder includes carry feedback.

Claim 2. The system of Claim 1 wherein said multiplier array includes a digit multiplier for each digit of at least one of said first operand and said second operand.

Claim 3. The system of Claim 1 wherein said first operand is a multiplicand and said second operand is a multiplier.

Claim 4. The system of Claim 1 wherein said wherein said recoded first operand and said recoded second operand are further partitioned in each digit multiplier to separate digits corresponding to at least one of sign, zero, one, and two to reduce the total number of combinations of digits for said recoded first operand and said recoded second operand.

Claim 5. The system of Claim 1 wherein said partial product is generated and accumulated every cycle for said selected digit and a particular digit of said recoded second operand.

Claim 6. The system of Claim 1 wherein said digit multiplier includes a negative sum converter configured to facilitate generating said sum by partitioning said partial product and ensuring a least significant digit thereof remains positive.

Claim 7. The system of Claim 1 wherein said and said partial product terms are added to an accumulation of previous partial product terms shifted one digit right such that a least significant digit shifted off is preserved as a result digit in said results register.

Claim 8. The system of Claim 1 wherein said partial product comprises a signed BCD carry digit and a signed BCD sum digit.

Claim 9. The system of Claim 1 wherein said partial product comprises a signed BCD carry digit and a positive BCD sum digit.

Claim 10. The system of Claim 1 wherein said multiplier array of digit multipliers generates an entire partial product for each digit of said recoded first operand in each multiplication cycle, said each multiplication cycle corresponding to a selected digit of said recoded second operand.

Claim 11. The system of Claim 1 wherein said carry feedback includes a carry out of said adder is shifted into a most significant digit to be accumulated with said sum.

Claim 12. A method for decimal multiplication comprising:

recoding decimal digits of a first operand to a corresponding set of {-5 to +5};

recoding decimal digits of a second operand to a corresponding set of {-5 to +5};

generating a partial product of a selected digit of a recoded first operand and a recoded second operand with a multiplier array of digit multipliers; and

accumulating a sum of said partial products with an adder array of digit adders, wherein a least significant digit of said sum is shifted to a results register, and each adder including carry feedback.

Claim 13. The method of Claim 12 wherein said multiplier array includes a digit multiplier for each digit of at least one of said first operand and said second operand.

Claim 14. The method of Claim 12 wherein said first operand is a multiplicand and said second operand is a multiplier.

Claim 15. The method of Claim 12 further including partitioning said recoded first operand and said recoded second operand to separate digits corresponding to at least one of sign, zero, one, and two to reduce the total number of combinations of digits for said recoded first operand and said recoded second operand.

Claim 16. The method of Claim 12 wherein said generating said partial product and accumulating a sum is completed every cycle for said selected digit and a particular digit of said recoded second operand.

Claim 17. The method of Claim 12 further including partitioning said partial product and ensuring a least significant digit thereof remains positive to facilitate said accumulating.

Claim 18. The method of Claim 12 wherein said accumulating includes adding said partial product terms to an accumulation of previous partial product terms shifted one digit right such that a least significant digit shifted off is preserved as a result digit in said results register.

Claim 19. The method of Claim 12 wherein said partial product comprises a signed BCD carry digit and a signed BCD sum digit.

Claim 20. The method of Claim 12 wherein said partial product comprises a signed BCD carry digit and a positive BCD sum digit.

Claim 21. The method of Claim 12 wherein said generating forms an entire partial product for each digit of said recoded first operand in each multiplication cycle,

said each multiplication cycle corresponding to a selected digit of said recoded second operand.

Claim 22. The method of Claim 12 wherein said carry feedback includes shifting a carry out into a most significant digit to be accumulated in said sum.

Claim 23. A system for decimal multiplication in a microprocessor comprising:

a means for recoding decimal digits of a first operand to a corresponding set of {-5 to +5};

a means for recoding decimal digits of a second operand to a corresponding set of {-5 to +5};

a means for generating a partial product of a selected digit of a recoded first operand and a recoded second operand with a multiplier array of digit multipliers; and

a means for accumulating a sum of said partial products with an adder array of digit adders, wherein a least significant digit of said sum is shifted to a results register, and each adder including carry feedback.

Claim 24. The system of Claim 23 wherein said multiplier array includes a digit multiplier for each digit of at least one of said first operand and said second operand.

Claim 25. The system of Claim 23 further including a means for partitioning said recoded first operand and said recoded second operand to separate digits corresponding to at least one of sign, zero, one, and two to reduce the total number of combinations of digits for said recoded first operand and said recoded second operand.

Claim 26. The system of Claim 23 further including a means for partitioning said partial product and ensuring a least significant digit thereof remains positive to facilitate said accumulating.

Claim 27. The system of Claim 23 wherein said means for accumulating includes a means for adding said partial product terms to an accumulation of previous

partial product terms shifted one digit right such that a least significant digit shifted off is preserved as a result digit in said results register.

Claim 28. The system of Claim 23 wherein said means for generating forms an entire partial product for each digit of said recoded first operand in each multiplication cycle, said each multiplication cycle corresponding to a selected digit of said recoded second operand.

Claim 29. The system of Claim 23 wherein said carry feedback includes a means for shifting a carry out into a most significant digit to be accumulated in said sum.